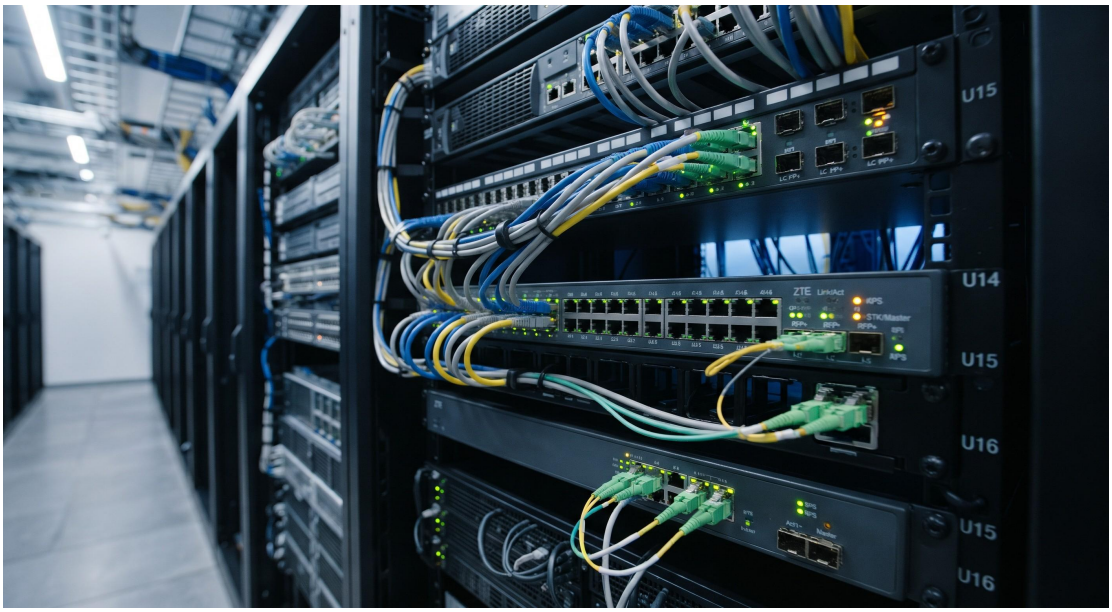
Ultra-Low Latency Packet Buffering Engine Factsheet: ZTE ZXR10 5250 Managed Switch Packet Buffer Memory Architecture

DESIGN PHILOSOPHY

The ZTE ZXR10 5250 Series represents a deliberate engineering approach to packet buffer memory allocation within a compact 1RU fixed-form-factor switching platform. Rather than treating buffer memory as a passive reservoir, the 5250 architecture employs a centralized high-speed ASIC forwarding engine that tightly couples on-chip packet buffering with line-rate Gigabit Ethernet processing . This design philosophy prioritizes deterministic behavior under bursty traffic conditions while maintaining the low power envelope and thermal simplicity required for carrier access and campus edge deployments. The packet buffer serves as the critical elasticity point between ingress port contention and egress scheduling, ensuring that short-term microbursts do not translate into avoidable tail-drop events.



PACKET BUFFER RETENTION DYNAMICS

The ZXR10 5250 utilizes an integrated switch chip with on-die packet memory, architecturally positioned to support simultaneous wire-speed forwarding across all Gigabit interfaces. The buffer subsystem operates in conjunction with a 16K-entry MAC address table and a 4K VLAN space, enabling the forwarding engine to maintain separate queue structures per port and per priority level . This queuing granularity is essential for preserving voice and video traffic during congestion events. The buffer allocation logic dynamically adjusts thresholds based on egress queue occupancy, allowing the switch to absorb transient bursts without prematurely discarding frames destined for less-congested ports. For access-layer scenarios where uplink oversubscription is common, the packet buffer effectively decouples ingress burst absorption from egress scheduling decisions, maintaining forwarding integrity even when

multiple downstream nodes transmit simultaneously toward a single aggregation uplink.

ENTERPRISE SOURCING ADVANTAGES

- Burst Absorption Without Head-of-Line Blocking: On-chip packet buffer memory isolates ingress contention domains, preventing a single congested egress port from degrading throughput on unrelated interfaces.
- Deterministic Tail-Drop Behavior: Buffer threshold management is calibrated to the 5250's line-rate forwarding capacity of up to 104 Gbps switching bandwidth on high-density models, ensuring that drop decisions occur only after available elasticity is genuinely exhausted .
- Power-Efficient Buffer Operation: The integrated ASIC approach eliminates discrete external buffer memory components, reducing PCB complexity, power draw, and thermal load compared to distributed buffer architectures.
- Seamless Integration with QoS Scheduling: The buffer subsystem interoperates directly with SP, WRR, and SP+WRR queue scheduling mechanisms, allowing priority traffic to access reserved buffer resources during congestion .

CERTIFICATIONS MATRIX

- IEEE 802.3af / 802.3at: Power over Ethernet and PoE+ support on designated models, with buffer memory prioritizing voice and AP uplink traffic under power-constrained conditions.

- IEEE 802.3az: Energy Efficient Ethernet compliance, with buffer state awareness enabling port sleep transitions during idle periods .

- IEEE 802.1Q: VLAN tagging and 4K VLAN support, with per-VLAN buffer accounting for traffic isolation.

- ITU-T G.8032 / RFC 3619: Ethernet ring protection with sub-50ms convergence, where buffer behavior during topology transitions preserves in-flight frames to the extent permitted by available memory .

- RoHS / WEEE / ISO 14001: Environmental compliance across the entire product lifecycle, including ASIC packaging and PCB assembly .

EXACT SPECS

TECHNICAL SPECIFICATIONS

Parameter | Specification

Form Factor | 1RU fixed-configuration chassis, 442 × 220 × 43.6 mm (typical)

Switching Capacity | Up to 104 Gbps (5250-52TC model); 56 Gbps (28-port models); 24 Gbps (12-port models)

Packet Forwarding Rate | Up to 78 Mpps (52-port models); 42 Mpps (28-port

models); 18 Mpps (12-port models)

Packet Buffer Architecture | Integrated on-chip shared memory within the switching ASIC; dynamic threshold allocation per egress queue

MAC Address Table | 16K entries

VLAN Capacity | 4K VLANs (IEEE 802.1Q), including Voice VLAN, PVLAN, and QinQ

QoS Queues | 8 priority queues per port; SP, WRR, and SP+WRR scheduling; tail-drop congestion avoidance

Jumbo Frame Support | Up to 10 KB

Power Supply | AC 100–240V, 50/60 Hz; optional DC/RPS input on select models

Maximum Power Consumption | <14.6W (12-port non-PoE); <53W (52-port non-PoE); PoE models vary by load

Operating Temperature | -5°C to +50°C

Reliability | MTBF > 100,000 hours; MTTR < 30 minutes

Parameter	**Specification**
Form Factor	1RU fixed-configuration chassis (442 × 220 × 43.6 mm typical)
Switching Capacity	Up to 104 Gbps (52-port models); 56 Gbps (28-port); 24 Gbps (12-port)
Packet Buffer	Integrated on-chip shared memory with dynamic per-queue threshold

	allocation
Forwarding Rate	Up to 78 Mpps (52-port); 42 Mpps (28-port); 18 Mpps (12-port)
MAC Address Table	16K entries
VLAN Support	4K VLANs (802.1Q), Voice VLAN, PVLAN, QinQ
QoS Scheduling	8 queues/port; SP, WRR, SP+WRR; tail-drop avoidance
Power Supply	AC 100 – 240V; dual redundant RPS option on select models
Max Power Consumption	<14.6W (12-port non-PoE); <53W (52-port non-PoE); PoE models load-dependent
Operating Temperature	-5°C to +50°C
MTBF	>100,000 hours

NETWORK ROI MATRIX

The packet buffer architecture of the ZXR10 5250 directly influences total cost of ownership in access and small-aggregation roles. By maintaining wire-speed forwarding under realistic burst conditions without external buffer memory, the

platform reduces component count, lowers field failure probability, and simplifies sparing logistics. For carrier access deployments where hundreds of subscriber lines converge onto Gigabit uplinks, the integrated buffer prevents unnecessary retransmissions at higher protocol layers, preserving application-layer throughput and reducing helpdesk escalations related to intermittent video stalls or VoIP jitter. The buffer's interaction with 802.3az EEE further reduces operational power costs by allowing idle ports to enter low-power states without flushing queued frames prematurely. In enterprise campus environments, the 5250's buffer behavior aligns with the predictable latency requirements of IP telephony and building automation traffic, enabling network managers to deploy a single switch family across wiring closets without segmenting latency-sensitive endpoints onto separate hardware.

